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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/814,173	04/01/2004	Shyh-Hsing Wang	3313-1143PUS1	7367

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EXAMINER	
CRUZ, IRIANA	

ART UNIT	PAPER NUMBER
2625	

NOTIFICATION DATE	DELIVERY MODE
09/08/2008	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

mailroom@bskb.com

Office Action Summary	Application No.	Applicant(s)	
	10/814,173	WANG ET AL.	
	Examiner	Art Unit	
	IRIANA CRUZ	2625	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 May 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15,18 and 19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15 and 18-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments with respect to claims 1-15 and 18-19 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

1. **Claims 1, 5-7 and 9-10** are rejected under 35 U.S.C. 103(a) as being unpatentable over Yoshito (JP Publication Number 2002-027249) in view of Burgess et al. (US Publication Number 2004/0131115 A1).

Regarding **Claim 1**, Yoshito'249 shows a memory management method for error diffusion comprising the steps of: dividing an image to be processed into a plurality of blocks **(i.e., an input image is divided into blocks side by side. See Paragraph 11 and See Figure 2)**; filling an initial region of a block according to an error diffusion method **(i.e., the blocks are generated/filled with error diffusion to near block of each block ((in order from first to last)). See Paragraph 11)**; performing error diffusion in order for each of the pixels in the block **(i.e., blocks contain pixels and the error diffusion is calculated in the blocks. See Paragraphs 11-12)**; and performing the error diffusion method for each of the blocks to complete halftone processing **(i.e., half toning equipment made to perform error diffusion. See Paragraph 13)**.

Yoshito'249 (although it shows the division of blocks and the error diffusion processing) fails to teach a method for reserving the pixels that are not processed in the final region of the block to the next adjacent block for later processing.

Burgess'115 teaches a method for reserving the pixels that are not processed in the final region of the block to the next adjacent block for later processing **(i.e., the image data is divided in blocks, each blocks unprocessed pixels are use to create the next block ((starting the adjacent block)) for later processing. See Paragraphs 94, 135-137)**.

Having the system of Yoshito'249 and then given the well-established teaching of the Burgess'115, it would have been obvious to one having ordinary skill in the art at the time of the invention was made to modify the system as suggested by the combination of Yoshito'249 with the teachings of Burgess'115 by adding to the block method the option of saving unprocessed pixels to start forming the next block to be processed, in order to improve the systems efficiency.

Regarding **Claim 5**, Yoshito'249 shows a method wherein the step of dividing an image to be processed into a plurality of blocks divides the image into a plurality of arrayed blocks **(i.e., an input image is divided into blocks side by side. See Paragraph 11 and See Figure 2)**.

Regarding **Claim 6**, Yoshito'249 shows a method wherein the arrayed blocks are regular rectangular blocks **(i.e., the input image is divided into rectangular block. See Paragraph 14)**.

Regarding **Claim 7**, Yoshito'249 shows a method wherein the step of dividing an image to be processed into a plurality of blocks divides according to the error diffusion method **(i.e., the image is divide in blocks where each block has its error diffusion calculated to the near block henceforth. See Paragraph 11-13)**.

Regarding **Claim 9**, Yoshito'249 shows a method wherein the step of filling an initial region of a block according to an error diffusion method filling the initial region of the block with required image data so that the pixels in the initial region are to be error diffused **(i.e., error diffusion is performed in each block and is offset to the next one following an order. See Paragraphs 12-13, 32 and 51)**.

Regarding **Claim 10**, Yoshito'249 shows a method wherein the image data being filled are pixels that are not processed in its adjacent blocks **(i.e., the blocks are filled in order, the pixels that did not made it into the previous block will be used to fill the next block. See Paragraphs 32 and 51)**.

2. **Claim 2-4, 8 and 11-15 and 18-19** are rejected under 35 U.S.C. 103(a) as being unpatentable over Yoshito (JP Publication Number 2002-027249) in view of Burgess et al. (US Publication Number 2004/0131115 A1), and further in view of Hattori (US Publication Number 2003/0123093).

The combination of Yoshito'249 and Burgess'115 fails to specify a method wherein the size of each divided block is smaller than the size of memory.

Hattori'093 teaches a method wherein the size of each divided block is smaller than the size of memory **(i.e., the tiles/blocks are stored in a memory, in order to be saved they have to be smaller in size than the memory. See Paragraph 31)**.

Having the system of Yoshito'249 and Burgess'115 and then given the well-established teaching of the Hattori'093, it would have been obvious to one having ordinary skill in the art at the time of the invention was made to modify the system of Yoshito'249 and Burgess'115 as taught by the Hattori'093, since using it reduces the

moiré fringes and enable expression of high-quality multiple gradations for halftoning method as suggested in reference Hattori'093 Paragraph 10.

Regarding **Claim 3**, the combination of Yoshito'249, Burgess'115 and Hattori'093 shows a method wherein the memory is an internal memory of an image processing chip **(i.e., halftoning circuit with internal memory. See Paragraph 145 in reference Hattori'093)**.

Regarding **Claim 4**, the combination of Yoshito'249, Burgess'115 and Hattori'093 teaches a method wherein the internal memory is static random access memory (SRAM) **(i.e., the internal memory used is an SRAM. See Paragraph 145 in reference Hattori'093)**.

Regarding **Claim 8**, the combination of Yoshito'249, Burgess'115 and Hattori'093 shows a method wherein the block is an approximately zigzag shape **(i.e., a virtual tile ((division blocks)) is provided with different shapes/zigzag. See Paragraphs 31, 89 and 93 and See Figures 2Cand 2D in reference Hattori'093)**.

Regarding **Claim 9**, the combination of Yoshito'249, Burgess'115 and Hattori'093 shows a method wherein the image data being filled are empty pixels **(i.e., some blocks are filled with empty pixels. See Paragraph 9 and See Figure 3A and 3B in reference Hattori'093)**.

Regarding **Claim 12**, Yoshito'249 shows a halftone processing module for error diffusion **(i.e., halftoning equipment to perform error diffusion. See Paragraph 13)** for dividing an image into a plurality of blocks **(i.e., an input image is divided into blocks side by side. See Paragraph 11 and See Figure 2)** and using an error

diffusion method to perform halftone processing **(i.e., halftoning equipment to perform error diffusion. See Paragraph 13)**, the module comprising: an image processing chip, which executes the error diffusion **(i.e., the halftoning equipment executes the error diffusion. See Paragraphs 13)**.

Yoshito'249 fails to show the method where the filling image data being all pixels not processed in the final region of the block to the next adjacent block.

Burgess'115 teaches the method where the filling image data being all pixels not processed in the final region of the block to the next adjacent block **(i.e., the image data is divided in blocks, each blocks unprocessed pixels are use to create the next block ((starting the adjacent block)) for later processing. See Paragraphs 94, 135-137)**.

Having the system of Yoshito'249 and then given the well-established teaching of the Burgess'115, it would have been obvious to one having ordinary skill in the art at the time of the invention was made to modify the system as suggested by the combination of Yoshito'249 with the teachings of Burgess'115 by adding to the block method the option of saving unprocessed pixels to start forming the next block to be processed, in order to improve the systems efficiency.

The combination of Yoshito'249 and Burgess'115 fails to show an internal memory which is inside the chip to store the block to be processed and the image data filling in the initial region of the block, and an external memory, which is outside the chip for providing the internal memory with the pixels needed to fill the block.

Hattori'093 teaches an internal memory which is inside the chip to store the block

to be processed and the image data filling in the initial region of the block **(i.e., halftoning circuit with internal memory. See Paragraph 145 in reference Hattori'093)** and an external memory, which is outside the chip for providing the internal memory with the pixels needed to fill the block **(i.e., pixels are load from external image memory. See Paragraph 145)**.

Having the system of Yoshito'249 and Burgess'115 and then given the well-established teaching of the Hattori'093, it would have been obvious to one having ordinary skill in the art at the time of the invention was made to modify the system of Yoshito'249 and Burgess'115 as taught by the Hattori'093, since using it reduces the moiré fringes and enable expression of high-quality multiple gradations for halftoning method as suggested in reference Hattori'093 Paragraph 10.

Regarding **Claim 13**, the combination of Yoshito'249, Burgess'115 and Hattori'093 teaches a halftone processing module wherein the internal memory is static random access memory (SRAM) **(i.e., the internal memory used is an SRAM. See Paragraph 145 in reference Hattori'093)**.

Regarding **Claim 14**, the combination of Yoshito'249,Burgess'115 and Hattori'093 shows the halftone processing module wherein the block to be processed has an approximately zigzag shape according to the error diffusion method **(i.e., a virtual tile ((division blocks)) is provided with different shapes/zigzag. See Paragraphs 31,89 and 93 and See Figures 2C and 2D in reference Hattori'093)**.

Regarding **Claim 15**, the combination of Yoshito'249, Burgess'115 and Hattori'093 shows the halftone processing module wherein the image data filling in the

initial region of the block are the image data that enable all the pixels in the initial region to be error diffused according to the error diffusion method **(i.e., error diffusion is performed in each block and is offset to the next one following an order. See Paragraphs 12-13, 32 and 51 in reference Yoshito'249)**.

Regarding **Claim 18**, the combination of Yoshito'249, Burgess'115 and Hattori'093 show a halftone processing module wherein the image data being filled are empty pixels. Hattori'093 teaches a halftone, processing module wherein the image data being filled are empty pixels **(i.e., some blocks are filled with empty pixels. See Paragraph 9 and See Figure 3A and 3B in reference Hattori'093)**.

Regarding **Claim 19**, the combination of Yoshito'249, Burgess'115 and Hattori'093 shows a halftone processing module wherein the external memory is dynamic random access memory (DRAM) **(i.e., the external image memory is an DRAM. See Paragraph 145 in reference Hattori'093)**.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to IRIANA CRUZ whose telephone number is (571)270-3246. The examiner can normally be reached on Monday-Friday 7:30am to 4:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, King Y. Poon can be reached on (571) 272-7440. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/King Y. Poon/
Supervisory Patent Examiner, Art Unit 2625

Iriana Cruz
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September 1, 2008

/I. C./
Examiner, Art Unit 2625